



# REPLACEMENT SHEET

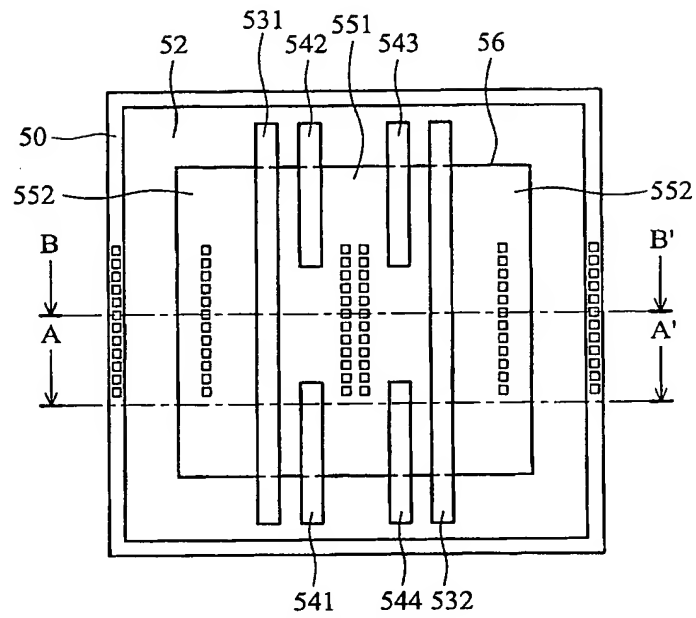


FIG. 5A

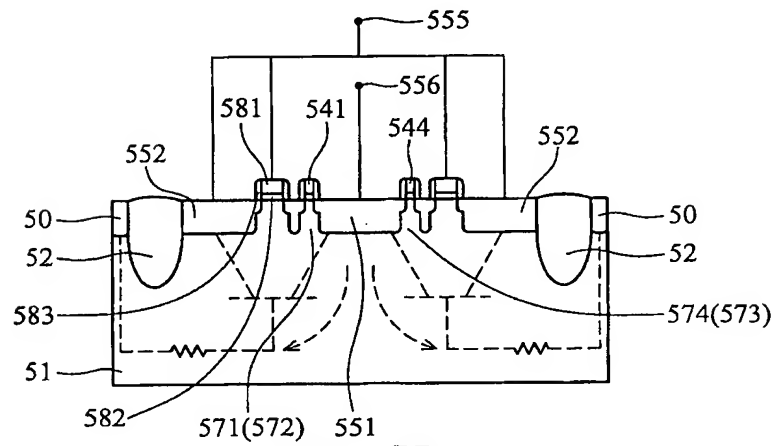


FIG. 5B

# REPLACEMENT SHEET

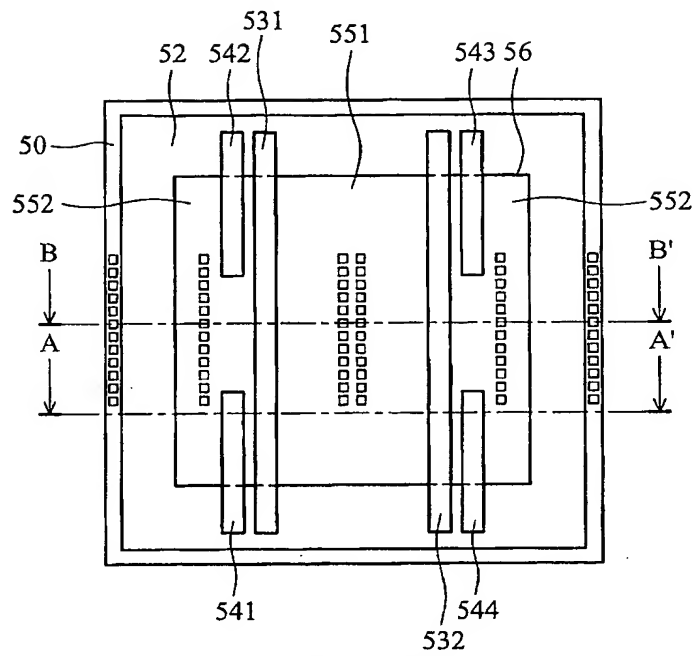


FIG. 6A

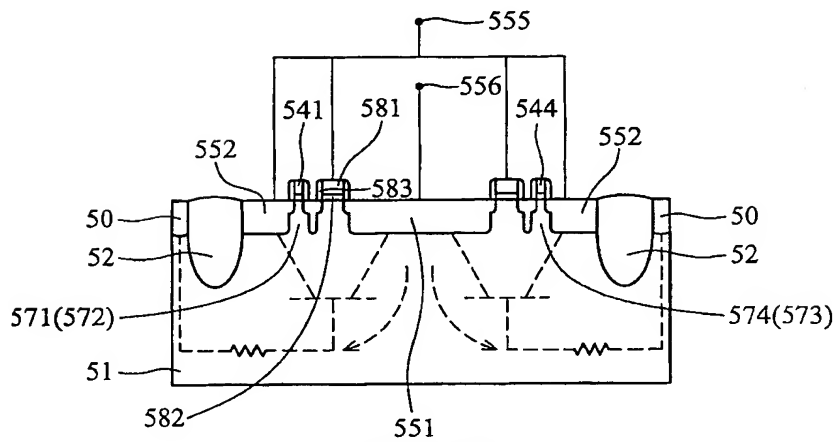


FIG. 6B

FIG. 1 is a schematic diagram of a multi-layer printed circuit board (PCB) layout. The diagram shows a central rectangular area (752) surrounded by a border (70). Within the central area, there are two vertical strips (731, 732) and two horizontal strips (741, 742). The strips are connected by a network of lines (743, 744). The entire structure is enclosed in a frame (76). Dimensions A and B are indicated on the left, and A' and B' are indicated on the right.

This diagram shows a cross-sectional view of a semiconductor device. A central channel region (751) is flanked by two side regions (752). The side regions are further divided into a top layer (70) and a bottom layer (72). A central gate structure (755) is positioned above the channel, with a gate electrode (756) and a gate insulator (781). The channel region is defined by a gate insulator (783) and a gate electrode (782). The side regions are separated from the channel by a barrier layer (741(742)). The bottom layer (72) contains a conductive layer (744(743)).

FIG. 7B

FIG. 8B

# REPLACEMENT SHEET

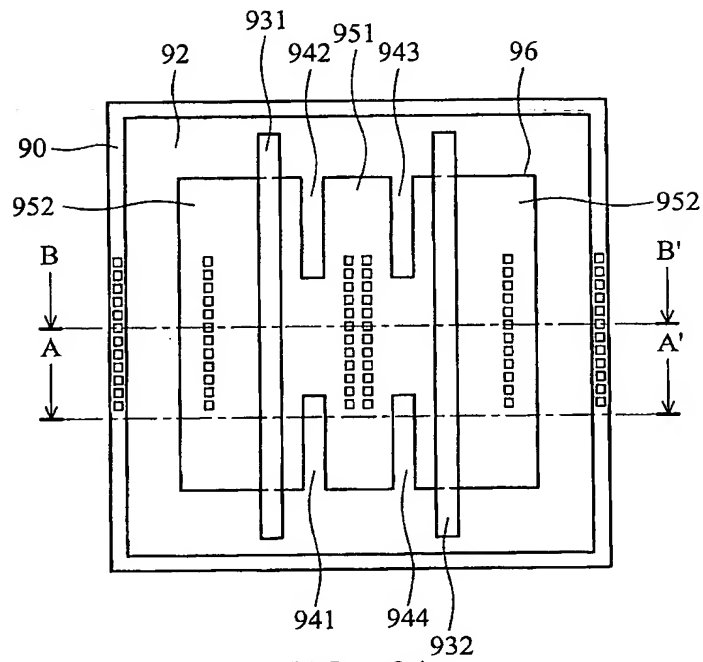


FIG. 9A

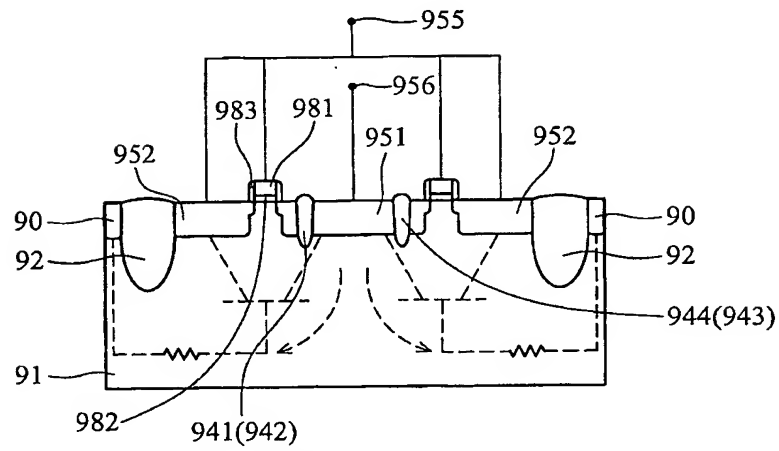


FIG. 9B

# REPLACEMENT SHEET

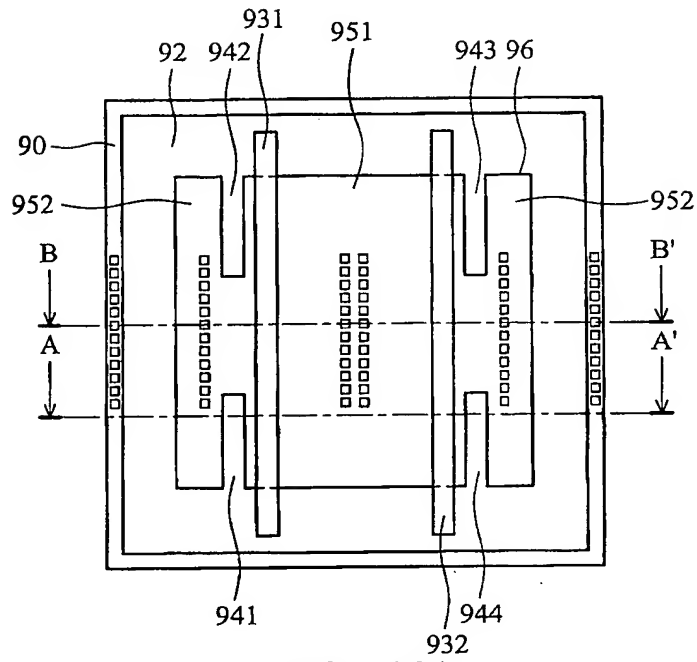


FIG. 10A

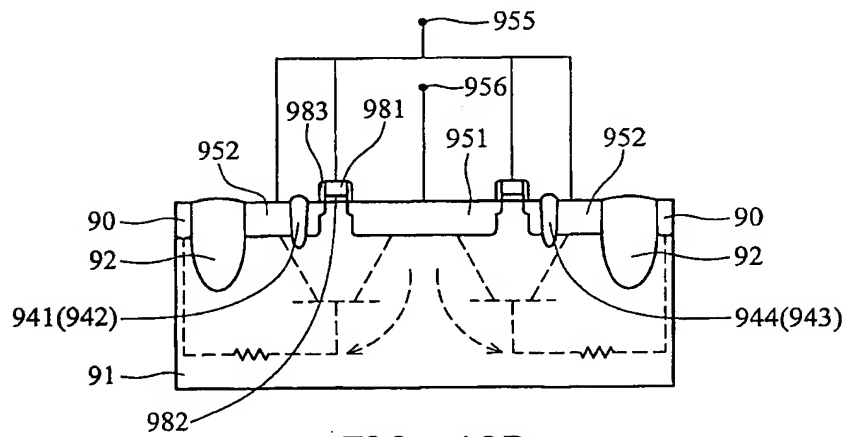


FIG. 10B

# REPLACEMENT SHEET

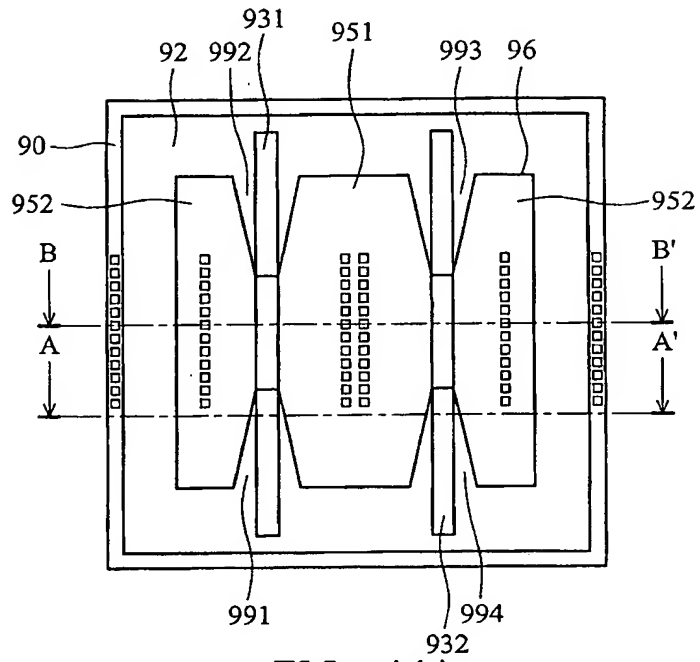


FIG. 11A

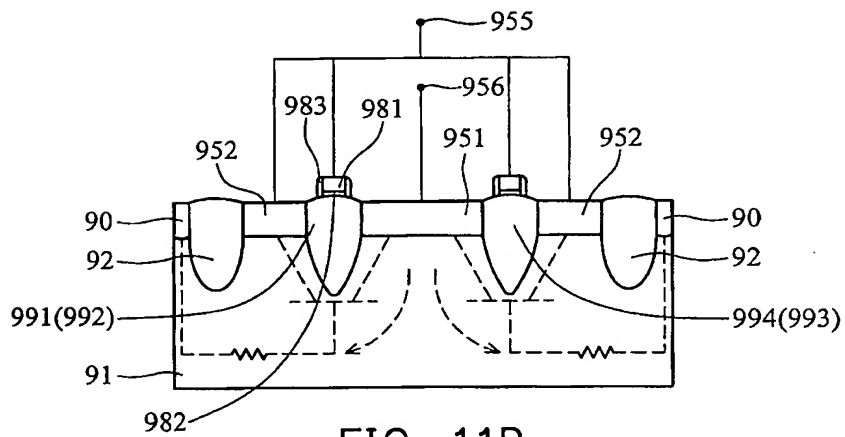


FIG. 11B

FIG. 12A

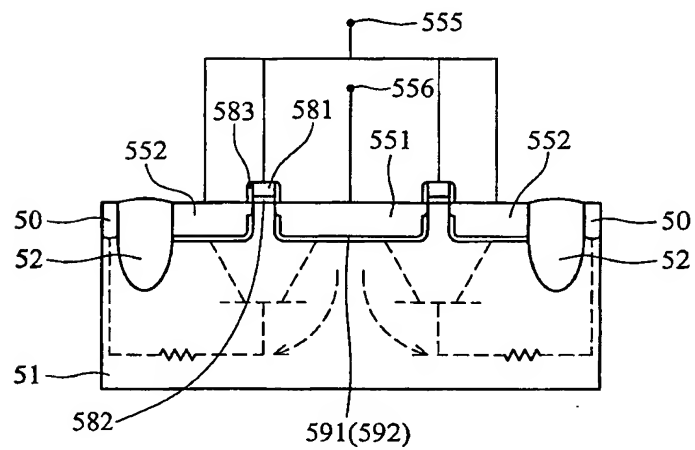


FIG. 12B

# REPLACEMENT SHEET

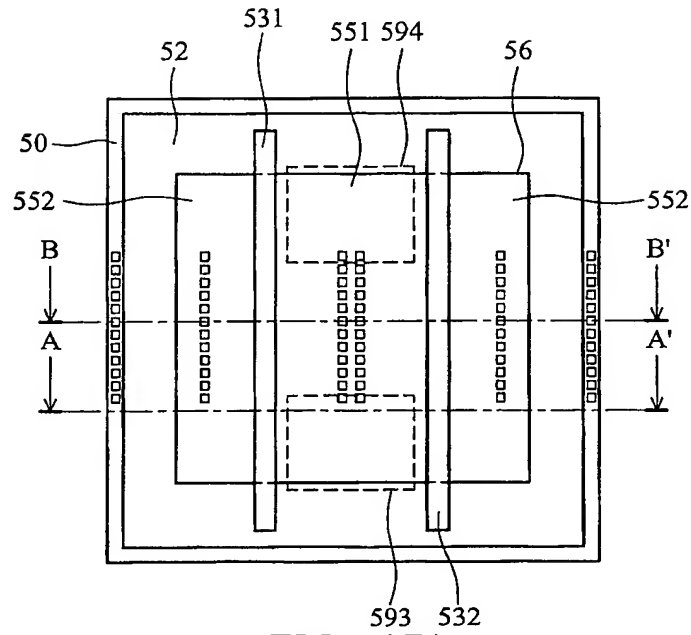


FIG. 13A

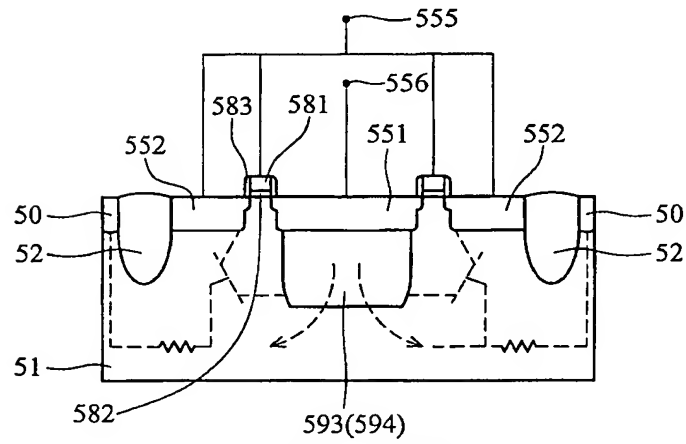


FIG. 13B

# REPLACEMENT SHEET

